

In the Abstract:

Please amend the abstract as follows:

The invention relates to a method of manufacturing a field effect transistor, in which ~~method~~ a semiconductor body (1) of silicon is provided at a surface thereof with a source region (2) and a drain region (3) of a first conductivity type, which regions are both provided with extensions (2A, 3A), and with a gate region (5) situated above the channel region. ~~A (4), and wherein a pn-junction is formed between the extensions (2A, 3A) and a neighboring part (4A) of the channel region (4) is formed by using an amorphizing implantation followed by two implantations (I₁, I₂) of dopants of opposite conductivity type, and wherein before said two implantations (I₁, I₂) of dopants of opposite conductivity type an amorphizing implantation (I₀) is performed where the pn-junction is to be formed. The amorphizing implantation (I₀) and said two implantations (I₁, I₂) of dopants are both carried out before the gate region (5) is formed and at an angle with the surface of the semiconductor body (1) which is substantially equal to 90 degrees. In this way, the most relevant part of the pn-junction formed, i.e. the ~~A steep and abrupt vertical part that runs perpendicularly to the surface, is not only very steep and abrupt but also has of the pn-junction is thus formed with~~ a very low leakage current due to the absence of implantations defects. Preferably In some embodiments, a low temperature anneal is used to regrow crystalline silicon.~~